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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,172	05/16/2005	Ramakrishman Venkata Subramanian	1890-0249	5743

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EXAMINER	
SCIACCA, SCOTT M	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/535,172	SUBRAMANIAN ET AL.	
	Examiner	Art Unit	
	Scott M. Sciacca	2146	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 11-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 11-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/26/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is responsive to communications filed on May 16, 2005. Claims 3-10 have been cancelled. Claims 1-2 and 11-23 are pending in the application.

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 11-12, 17-20 and 22-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Schnell (US 5,757,795).

Regarding Claim 1, Schnell teaches a data switch having a plurality of ingress/egress ports (Fig. 2 shows a plurality of I/O ports 104) and for transmitting data packets including a destination address (*"The header usually includes a source address identifying a data device originating the packet and a destination address identifying the destination data device"* – See Col. 5, lines 54-57), the data switch having address table construction means for generating a table containing associations between ports of the switch and MAC addresses of any devices connected to the switch via those ports (*"The*

MAC address map 412 is a linked list structure including each MAC address received and the corresponding port number associated with that MAC address" – See Col. 10, lines 64-66; *"The packet processor 212 receives all packets containing new MAC addresses, and updates the MAC address map 412 and the hash memory 217. A new source MAC address is copied into the MAC address map 412 along with its corresponding port number"* – See Col. 11, lines 21-25), the address table construction means being operable to construct said table in respect of all but a first one of the ports (*"A new source MAC address is copied into the MAC address map 412 along with its corresponding port number"* – See Col. 11, lines 23-25; A first port of the switch will not have an entry in the address table if a device connected to said port has not sent a packet to the switch or if there is no device connected to the port).

Regarding Claim 2, Schnell teaches the address table construction means being further operable to construct said table in respect of all of the ports, according to a setting of a control register (*"The memory 404 includes read-only memory (ROM) 408 for storing startup routines to initialize the processor 402 and run-time routines performed by the processor 402"* – See Col. 9, lines 43-46; *"The packet processor 212 receives all packets containing new MAC addresses, and updates the MAC address map 412 and the hash memory 217"* – See Col. 11, lines 21-23).

Regarding Claim 11, Schnell teaches an arrangement including a data switch for transmitting data packets including a destination address, the data switch comprising:

a first ingress/egress port and a plurality of other ingress/egress ports (Fig. 2 shows a plurality of I/O ports 104);

a table store configured to store a table containing associations between the plurality of other ingress/egress ports and MAC addresses of any devices connected to the switch via the plurality of other ingress/egress ports (*"The MAC address map 412 is a linked list structure including each MAC address received and the corresponding port number associated with that MAC address"* – See Col. 10, lines 64-66);

a switching fabric (*"The network switch further includes switching fabric with a switch controller for controlling transfer of data packets between the network ports and the packet buffers"* – See Col. 3, lines 2-4), and

a control unit operable to control the switching fabric (*"The network switch further includes switching fabric with a switch controller for controlling transfer of data packets between the network ports and the packet buffers"* – See Col. 3, lines 2-4), the control unit being arranged, upon receiving a data packet from any of the other ingress/egress ports having a destination address which is not stored in the table, to control the switching fabric to transmit the data packet to the first ingress/egress port (*"If the packet is a unicast packet and its destination MAC address is unknown, then the packet processor 212 replicates the packet to all of the other ioports 104 other than the input port"* – See Col. 11, lines 31-34; When the switch receives a packet from a port other than the first ingress/egress port and the destination MAC address of the packet is not listed in the address table, then the packet is forwarded to the first ingress/egress port).

Regarding Claim 12, Schnell teaches the first ingress/egress port being adapted to be connected to a communication network (Fig. 1 shows IOPORT2 connected to NETWORK2 via link 108).

Regarding Claim 17, Schnell teaches a method of operating a data switch comprising a first ingress/egress port and a plurality of other ingress/egress ports, the method including:

generating a table containing associations between at least the plurality of other ingress/egress ports of the switch and MAC addresses of any devices connected to the switch thereby (*"The packet processor 212 initializes the MAC address map 412 and the hash memory 217 upon power up"* – See Col. 11, lines 9-10),

stopping generation of the table before MAC addresses of at least some devices operably coupled through the first ingress/egress port are associated with the first ingress/egress port in the table (*"The packet processor 212 receives all packets containing new MAC addresses, and updates the MAC address map 412 and the hash memory 217. A new source MAC address is copied into the MAC address map 412 along with its corresponding port number"* – See Col. 11, lines 21-25; Generation stops and then continues once a packet is received which has a destination MAC address not listed in the table).

Regarding Claim 18, Schnell teaches stopping generation of the table occurring after at least one MAC address of at least one device operably coupled through the first ingress/egress port is associated with the first ingress/egress port in the table (*"The packet processor 212 receives all packets containing new MAC addresses, and updates the MAC address map 412 and the hash memory 217. A new source MAC address is copied into the MAC address map 412 along with its corresponding port number"* – See

Col. 11, lines 21-25; Generation of the address table stops when the switch does not receive any packets with destination MAC addresses that aren't listed in the table).

Regarding Claim 19, Schnell teaches receiving a data packet having a destination port MAC address absent from the generated table and forwarding the data packet to the first ingress/egress port (*"If the packet is a unicast packet and its destination MAC address is unknown, then the packet processor 212 replicates the packet to all of the other ioports 104 other than the input port"* – See Col. 11, lines 31-34; When the switch receives a packet from a port other than the first ingress/egress port and the destination MAC address of the packet is not listed in the address table, then the packet is forwarded to the first ingress/egress port).

Regarding Claim 20, Schnell teaches forwarding the data packet further comprising forwarding the data packet only if the data packet was received from one of the plurality of other ingress/egress ports (*"For example, if a unicast packet with an unknown destination MAC address is received at IOPORT1, then the packet processor 212 replicates the packet to IOPORT2"* – See Col. 11, lines 35-38).

Regarding Claim 22, Schnell teaches a method of operating a data switch for switching data packets including a destination address (*"The header usually includes a source address identifying a data device originating the packet and a destination address identifying the destination data device"* – See Col. 5, lines 54-57), the data switch comprising a first ingress/egress port, a plurality of other ingress/egress ports (Fig. 2 shows a plurality of I/O ports 104), and a memory storing a table containing associations between the other ingress/egress ports and MAC addresses of any

devices connected to the switch via the other ingress/egress ports (*"The memory 404 also includes DRAM 410 for storing parameters and data during run-time, and also an DRAM for storing a MAC address map 412 of all MAC addresses received at the ioports 104"* – See Col. 9, lines 46-49), the method comprising:

receiving a data packet from any of the other ingress output ports and transmitting the data packet to the first ingress/egress port if the data packet contains a destination address that is absent from the table (*"For example, if a unicast packet with an unknown destination MAC address is received at IOPORT1, then the packet processor 212 replicates the packet to IOPORT2"* – See Col. 11, lines 35-38).

Regarding Claim 23, Schnell teaches transmitting the data packet to a corresponding ingress/output port if the data packet contains a destination that is present on the table (*"A hash system for selecting a destination network port for each of a plurality of binary address values, such as media access control (MAC) addresses, received by a plurality of network ports including a hash memory for receiving binary hash values and for providing a corresponding port number identifying a destination network port"* – See Abstract).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 13-16 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schnell (US 5,757,795) as applied to Claims 11 and 17 above, and further in view of Kramer et al. (US 6,658,027).

Regarding Claim 13, Schnell does not explicitly teach at least one of the other ingress/egress ports being arranged to receive and transmit voice signals, but does disclose the switch being operable to receive and transmit Ethernet data (*"the Ethernet protocol includes a variety of data rates and speeds. Any particular data rate may be used at any particular ioport 104"* – See Col. 17, lines 40-44). Kramer teaches modulating voice signals into Ethernet data (Fig. 3 shows a VoIP apparatus which converts a voice signal via CODEC 160 to Ethernet data via Ethernet interface 310). It would have been obvious to one of ordinary skill in the art at the time the invention was made to convert voice signals to Ethernet data for use with the network switch disclosed by Schnell. Motivation for doing so would be to carry voice signals and other data over the same network infrastructure.

Regarding Claim 14, Kramer teaches the arrangement according to Claim 13 further comprising a microphone, a speaker, circuitry configured to transform sound signals received from the microphone into data packets and to transform data packets into control signals for the speaker (Fig. 3 shows a microphone, speaker, CODEC 160 and various other circuitry used to convert analog voice signals to digital packet data as well as convert digital packet data to audio signals for playback through a speaker), and wherein the circuitry is coupled to the at least one of the other ingress/egress ports arranged to receive and transmit voice signals (Fig. 3 shows Ethernet interface 310

which may be coupled one of the ingress/egress ports of the Ethernet switch disclosed by Schnell).

Regarding Claim 15, Schnell teaches sockets adapted to connect one or more of the other ingress/egress ports to devices which each have a MAC address (*"A network switch for transferring data packets according to the present invention includes a plurality of network ports, a plurality of packet buffers, and a switch matrix coupled to each of the network ports"* – See Col. 2, lines 63-66; *"In the specific embodiment described herein, the binary address values are media access control (MAC) addresses used for uniquely identifying network devices"* – See Col. 3, lines 29-31).

Regarding Claim 16, Schnell teaches the first ingress/egress port being adapted to be connected to a communications network (Fig. 1 shows IOPORT2 connected to NETWORK2 via link 108).

Regarding Claim 17, Kramer teaches converting analog audio signals to data packets (Fig. 3 shows a CODEC 160 for receiving analog audio data from a microphone and encoding the data into digital packet data) and providing the data packets to one of the other ingress/egress ports (Fig. Shows an Ethernet interface 310 for providing the packet data to one of the ingress/egress ports of the Ethernet switch disclosed by Schnell). It would have been obvious to one of ordinary skill in the art at the time the invention was made to convert voice signals to Ethernet data for use with the network switch disclosed by Schnell for the same reasons as those given with regard to Claim 13.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott M. Sciacca whose telephone number is (571) 270-1919. The examiner can normally be reached on Monday thru Friday, 7:30 A.M. - 5:00 P.M. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeff Pwu can be reached on (571) 272-6798. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

JEFFREY PWU
SUPERVISORY PATENT EXAMINER